



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE

United States Patent and Trademark Office

Address: COMMISSIONER FOR PATENTS

P.O. Box 1450

Alexandria, Virginia 22313-1450

www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/501,150	07/13/2004	Syuji Matsuda	2004_1091A	5201
513 7590 01/25/2011 WENDEROTH, LIND & PONACK, L.L.P. 1030 15th Street, N.W., Suite 400 East Washington, DC 20005-1503				
EXAMINER				
TORRES, JOSEPH D				
ART UNIT		PAPER NUMBER		
2112				
NOTIFICATION DATE		DELIVERY MODE		
01/25/2011		ELECTRONIC		

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ddalecki@wenderoth.com

coa@wenderoth.com



UNITED STATES PATENT AND TRADEMARK OFFICE

Commissioner for Patents  
United States Patent and Trademark Office  
P.O. Box 1450  
Alexandria, VA 22313-1450  
[www.uspto.gov](http://www.uspto.gov)

**BEFORE THE BOARD OF PATENT APPEALS  
AND INTERFERENCES**

Application Number: 10/501,150  
Filing Date: July 13, 2004  
Appellant(s): MATSUDA ET AL.

---

Kenneth W. Fields  
For Appellant

**EXAMINER'S ANSWER**

This is in response to the appeal brief filed 12/29/2010 appealing from the Office action mailed 04/19/2010.

**(1) Real Party in Interest**

The examiner has no comment on the statement, or lack of statement, identifying by name the real party in interest in the brief.

**(2) Related Appeals and Interferences**

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

**(3) Status of Claims**

The following is a list of claims that are rejected and pending in the application:

Claims 17, 19, 20, 22, 24 and 25 stand finally rejected under 35 U.S.C. § 103(a).

**(4) Status of Amendments After Final**

The examiner has no comment on the appellant's statement of the status of amendments after final rejection contained in the brief.

**(5) Summary of Claimed Subject Matter**

The examiner has no comment on the summary of claimed subject matter contained in the brief.

**(6) Grounds of Rejection to be Reviewed on Appeal**

The examiner has no comment on the appellant's statement of the grounds of rejection to be reviewed on appeal. Every ground of rejection set forth in the Office action from which the appeal is taken (as modified by any advisory actions) is being maintained by the examiner except for the grounds of rejection (if any) listed under the

subheading "WITHDRAWN REJECTIONS." New grounds of rejection (if any) are provided under the subheading "NEW GROUNDS OF REJECTION."

**(7) Claims Appendix**

The examiner has no comment on the copy of the appealed claims contained in the Appendix to the appellant's brief.

**(8) Evidence Relied Upon**

6,631,492	MARCHANT	10-2003
5,684,810	NAKAMURA et al	11-1997
6,029,264	KOBAYASHI et al	02-2000
7,089,401	SHUTOKU et al	08-2006
3,685,016	EACHUS	08-1972

**(9) Grounds of Rejection**

The following ground(s) of rejection are applicable to the appealed claims:

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.

2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 17, 19, 20, 22, 24 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Marchant; Alan B. (US 6631492 B2) in further view of Nakamura; Takahiko et al. (US 5684810 A, hereafter referred to as Nakamura) and Kobayashi; Hisashi et al. (US 6029264 A, hereafter referred to as Kobayashi; Note: Kobayashi is used strictly as a teaching reference).

Summary of the teachings in Marchant:

Col. 3, lines 30-59 in Marchant teaches using ECC product codeword to correct burst errors due to scratches. Figures 6 and 7 in Marchant teaches how the ECC product codeword of Figure 5 lines up with scratches on a recording media prior to being read and processed to recover the stored data. Note: Col. 4, lines 41-60 in Marchant teaches that the recorded code is a cross interleaved code so that Figures 5-7 shows how the inner codewords line up with scratches on a recording media prior to being read and processed to recover the stored data. Kobayashi is used a teaching reference for a cross interleaved code. Figure 2 in the Kobayashi teaching reference teaches that a cross interleaved codeword is generated by scrambling/interleaving an outer codeword and inner encoding the scrambled/interleaved outer codeword to generate an inner codewords as shown in Figure 5-6 of Marchant. Figure 2 in Kobayashi teaches that deinterleaving occurs after inner decoding a cross interleaved codeword.

35 U.S.C. 103(a) rejection of claims 17 and 22:

Marchant teaches an error correction method for an error correction code (ECC) block that includes Reed-Solomon-coded data said error correction method using a plurality of bytes of sub data which comprise error correction codes that are independent from error correction codes of an error correction target code line to configure erasure position information (col. 3, lines 30-59 in Marchant teaches using a plurality of pieces of inner/row codeword sub data which comprise error correction codes that are independent from error correction codes of an outer/column error correction target code line to configure erasure position information; Note: col. 3, lines 41-57 in Marchant teaches that inner/row codeword sub data of the product code is used to configure erasure position information), the plurality of bytes of sub data including at least a first byte of sub data and a second byte of sub data (Figure 7 of Marchant teaches that the plurality of bytes of sub data include at least a first byte of sub data 48b in inner/row codeword sub data row 3 of Figure 7 and a second byte of sub data 48a in inner/row codeword sub data row 3), said error correction method comprising:

judging whether or not a first byte of main data, which is one of a plurality of bytes of main data of the error correction target code line, and a second byte of main data, which is one of a plurality of bytes of main data of a previous error correction code line, were located between the first and second bytes of sub data before being deinterleaved (col. 6, lines 28-56 in Marchant teach judging whether or not a first piece of data 48b in inner/row codeword sub data row 3 of Figure 7, which is one of a plurality of pieces of

data of the outer/column error correction target code line 44b, and a second piece of data 48a in inner/row codeword sub data row 3, which is one of a plurality of pieces of data of a previous error correction code line 44a, were located between the same pieces of inner/row codeword sub data rows 2 to 4 before being deinterleaving; Note: Col. 4, lines 41-60 in Marchant teaches that the recorded code is a cross interleaved code so that Figures 5-7 shows how the inner codewords line up with scratches on a recording media prior to being read and processed to recover the stored data hence prior to being de-interleaved); configuring erasure position information of said first byte of main data belonging to the error correction target code line to be identical to erasure position information of said second byte of main data belonging to the previous error correction code line when said judging judges that the first byte of main data and the second byte of main data were both located between the first and second bytes of sub data before being deinterleaved (col. 6, lines 28-56 in Marchant teach that symbols in a scratch field are configured/flagged with erasure information for a scratch so that they are configured/flagged with erasure position information for the same scratch, in particular; this process is a step for configuring/flagging erasure position information of said first piece of data 48b belonging to the outer/column error correction target code line 44b to be the same as identical row position 3 to erasure position information of said second piece of data 48a belonging to the previous error correction code line 44a when said judgment step judging judges that the first piece of data 48b and the second piece of data 48a are both located between the same pieces of inner/row codeword sub data rows 2 to 4), the erasure position information being obtained at a time of

performing Reed-Solomon decoding on the Reed-Solomon-coded data (Col. 3, lines 41-47 in Marchant teaches that configuring/flagging with erasure position information occurs during inner decoding; Note: in cross interleaved codewords, inner decoding occurs before deinterleaving, e.g., Figure 2 in the Kobayashi teaching reference); and performing error correction on the error correction target code line (col. 6, lines 28-56 in Marchant).

As per additional limitations in claim 22: Col. 3, lines 41-47 in Marchant teaches that configuring/flagging with erasure position information occurs during inner decoding prior to de-interleaving.

However Marchant does not explicitly teach the specific use of erasure position information being obtained from a position polynomial. **Note: col. 3, lines 41-59 in Marchant teaches that C1 inner codeword rows exceeding error correction capabilities are flagged. An erasure flagged row within a C2 column outer code codeword is a position of an erroneous symbol within the C2 column outer code codeword. Hence, the erasure flag in Marchant provides error position information for a symbol within a C2 column/outer code codeword.**

Nakamura, in an analogous art, teaches the erasure position information being obtained from a position polynomial **(Col. 6, line 51 to col. 7, line 9 and Figure 5 in Nakamura teaches that during C1 inner decoding error location/position polynomials are generated in Block 3 and are used to generate feedback information to generate erasure information in Blocks 7, 7(b), 7(c) and 8; Specifically, col. 7, lines 2-5 in Nakamura teaches that error locations of the C1 inner/row error location/position**

polynomial are converted to erasure locations to be used in C2 outer/column error correction decoding whenever uncorrectable-error flags are output to Blocks 7, 7(b), 7(c) and 8, that is: the erasure position/location information stored in Block 8 is obtained from a error/position polynomial).

In summary, col. 6, line 61 to col. 7, line 8 in Nakamura teach that error locations of the C1 inner/row error location/position polynomial are converted to erasure locations to be used in C2 outer/column error correction decoding whenever uncorrectable-error flags are output to Blocks 7, 7(b), 7(c) and 8, which is substantially what is already taught in Marchant. Col. 6, line 6-17 of Marchant clearly suggests the use of a Reed-Solomon Erasure code. Nakamura teaches that in Reed-Solomon Erasure decoding erasures are erasure flagged during C1 inner/row code decoding just as in Marchant. However, Nakamura provides details missing in Marchant as to how erasure flagging is executed. Col. 6, line 51 to col. 7, line 9 and Figure 5 in Nakamura teaches that during C1 inner decoding error location/position polynomials are generated in Block 3 and are used to generate feedback information to generate erasure information in Blocks 7, 7(b), 7(c) and 8. Specifically, col. 7, lines 2-5 in Nakamura teaches that error locations of the C1 inner/row error location/position polynomial are converted to erasure locations to be used in C2 outer/column error correction decoding whenever uncorrectable-error flags are output to Blocks 7, 7(b), 7(c) and 8, that is: the erasure position/location information stored in Block 8 is obtained from a error/position polynomial).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Marchant with the teachings of Nakamura by including use of erasure position information being obtained from a position polynomial. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of erasure position information being obtained from a position polynomial would have provided a means for obtaining erasure information for inner C1 uncorrectable errors (col. 6, line 51 to col. 7, line 9 and Figure 5 in Nakamura).

35 U.S.C. 103(a) rejection of claims 19 and 24:

Marchant teaches an error correction method for an error correction code (ECC) block that includes Reed-Solomon-coded data said error correction method using a plurality of bytes of sub data which comprise error correction codes that are independent from error correction codes of an error correction target code line to configure erasure position information (col. 3, lines 30-59 in Marchant teaches using a plurality of pieces of inner/row codeword sub data which comprise error correction codes that are independent from error correction codes of an outer/column error correction target code line to configure erasure position information; Note: col. 3, lines 41-57 in Marchant teaches that inner/row codeword sub data of the product code is used to configure erasure position information), the plurality of bytes of sub data including at least a first byte of sub data and a second byte of sub data (Figure 7 of Marchant teaches that the plurality of bytes of sub data

include at least a first byte of sub data 48b in inner/row codeword sub data row 3 of Figure 7 and a second byte of sub data 48a in inner/row codeword sub data row 3), said error correction method comprising:

judging whether or not a first byte of main data, which is one of a plurality of bytes of main data of the error correction target code line, and a second byte of main data, which is one of a plurality of bytes of main data of a previous error correction code line, were located between the first and second bytes of sub data before being deinterleaved (col. 6, lines 28-56 in Marchant teach judging whether or not a first piece of data 48b in inner/row codeword sub data row 3 of Figure 7, which is one of a plurality of pieces of data of the outer/column error correction target code line 44b, and a second piece of data 48a in inner/row codeword sub data row 3, which is one of a plurality of pieces of data of a previous error correction code line 44a, were located between the same pieces of inner/row codeword sub data rows 2 to 4 before being deinterleaving; Note: Col. 4, lines 41-60 in Marchant teaches that the recorded code is a cross interleaved code so that Figures 5-7 shows how the inner codewords line up with scratches on a recording media prior to being read and processed to recover the stored data hence prior to being de-interleaved); configuring erasure position information of said first byte of main data belonging to the error correction target code line to be identical to erasure position information of said second byte of main data belonging to the previous error correction code line when said judging judges that the first byte of main data and the second byte of main data were both located between the first and second bytes of sub data before being deinterleaved (col. 6, lines 28-56 in Marchant teach that symbols in a

scratch field are configured/flagged with erasure information for a scratch so that they are configured/flagged with erasure position information for the same scratch, in particular; this process is a step for configuring/flagging erasure position information of said first piece of data 48b belonging to the outer/column error correction target code line 44b to be the same as identical row position 3 to erasure position information of said second piece of data 48a belonging to the previous error correction code line 44a when said judgment step judging judges that the first piece of data 48b and the second piece of data 48a are both located between the same pieces of inner/row codeword sub data rows 2 to 4), the erasure position information being obtained at a time of performing Reed-Solomon decoding on the Reed-Solomon-coded data (Col. 3, lines 41-47 in Marchant teaches that configuring/flagging with erasure position information occurs during inner decoding; Note: in cross interleaved codewords, inner decoding occurs before deinterleaving, e.g., Figure 2 in the Kobayashi teaching reference); and performing error correction on the error correction target code line (col. 6, lines 28-56 in Marchant).

As per additional limitations in claim 24: Col. 3, lines 41-47 in Marchant teaches that configuring/flagging with erasure position information occurs during inner decoding prior to de-interleaving.

However Marchant does not explicitly teach the specific use of erasure position information being obtained from a position polynomial. **Note: col. 3, lines 41-59 in Marchant teaches that C1 inner codeword rows exceeding error correction capabilities are flagged. An erasure flagged row within a C2 column outer code**

codeword is a position of an erroneous symbol within the C2 column outer code codeword. Hence, the erasure flag in Marchant provides error position information for a symbol within a C2 column/outer code codeword.

Nakamura, in an analogous art, teaches the erasure position information being obtained from a position polynomial (Col. 6, line 51 to col. 7, line 9 and Figure 5 in Nakamura teaches that during C1 inner decoding error location/position polynomials are generated in Block 3 and are used to generate feedback information to generate erasure information in Blocks 7, 7(b), 7(c) and 8; Specifically, col. 7, lines 2-5 in Nakamura teaches that error locations of the C1 inner/row error location/position polynomial are converted to erasure locations to be used in C2 outer/column error correction decoding whenever uncorrectable-error flags are output to Blocks 7, 7(b), 7(c) and 8, that is; the erasure position/location information stored in Block 8 is obtained from a error/position polynomial).

In summary, col. 6, line 61 to col. 7, line 8 in Nakamura teach that error locations of the C1 inner/row error location/position polynomial are converted to erasure locations to be used in C2 outer/column error correction decoding whenever uncorrectable-error flags are output to Blocks 7, 7(b), 7(c) and 8, which is substantially what is already taught in Marchant. Col. 6, line 6-17 of Marchant clearly suggests the use of a Reed-Solomon Erasure code. Nakamura teaches that in Reed-Solomon Erasure decoding erasures are erasure flagged during C1 inner/row code decoding just as in Marchant. However, Nakamura provides details missing in Marchant as to how erasure flagging is executed. Col. 6, line

51 to col. 7, line 9 and Figure 5 in Nakamura teaches that during C1 inner decoding error location/position polynomials are generated in Block 3 and are used to generate feedback information to generate erasure information in Blocks 7, 7(b), 7(c) and 8. Specifically, col. 7, lines 2-5 in Nakamura teaches that error locations of the C1 inner/row error location/position polynomial are converted to erasure locations to be used in C2 outer/column error correction decoding whenever uncorrectable-error flags are output to Blocks 7, 7(b), 7(c) and 8, that is: the erasure position/location information stored in Block 8 is obtained from a error/position polynomial).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Marchant with the teachings of Nakamura by including use of erasure position information being obtained from a position polynomial. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of erasure position information being obtained from a position polynomial would have provided a means for obtaining erasure information for inner C1 uncorrectable errors (col. 6, line 51 to col. 7, line 9 and Figure 5 in Nakamura).

Sub data 48a and 48b in Figure 7 of Marchant is sync data for configuring/flagging erasures.

35 U.S.C. 102(e) rejection of claims 20 and 25.

If first data is outside of sub data 48a and 48b in Figure 7 of Marchant, then it does not exist within sub data 48a and 48b.

Claims 18, 23, 37 and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Marchant; Alan B. (US 6631492 B2) in further view of Nakamura; Takahiko et al. (US 5684810 A, hereafter referred to as Nakamura) and Kobayashi; Hisashi et al. (US 6029264 A, hereafter referred to as Kobayashi; Note: Kobayashi is used strictly as a teaching reference) in further view of Shutoku; Toshiyuki et al. (US 7089401 B2, hereafter referred to as Shutoku).

35 U.S.C. 103(a) rejection of claims 18 and 23.

Marchant teaches an error correction method for an error correction code (ECC) block that includes Reed-Solomon-coded data said error correction method using a plurality of bytes of sub data which comprise error correction codes that are independent from error correction codes of an error correction target code line to configure erasure position information (col. 3, lines 30-59 in Marchant teaches using a plurality of pieces of inner/row codeword sub data which comprise error correction codes that are independent from error correction codes of an outer/column error correction target code line to configure erasure position information; Note: col. 3, lines 41-57 in Marchant teaches that inner/row codeword sub data of the product code is used to configure erasure position information),

the plurality of bytes of sub data including at least a first byte of sub data and a second byte of sub data (Figure 7 of Marchant teaches that the plurality of bytes of sub data include at least a first byte of sub data 48b in inner/row codeword sub data row 3 of Figure 7 and a second byte of sub data 48a in inner/row codeword sub data row 3), said error correction method comprising:

judging whether or not a first byte of main data, which is one of a plurality of bytes of main data of the error correction target code line, and a second byte of main data, which is one of a plurality of bytes of main data of a previous error correction code line, were located between the first and second bytes of sub data before being deinterleaved (col. 6, lines 28-56 in Marchant teach judging whether or not a first piece of data 48b in inner/row codeword sub data row 3 of Figure 7, which is one of a plurality of pieces of data of the outer/column error correction target code line 44b, and a second piece of data 48a in inner/row codeword sub data row 3, which is one of a plurality of pieces of data of a previous error correction code line 44a, were located between the same pieces of inner/row codeword sub data rows 2 to 4 before being deinterleaving; Note: Col. 4, lines 41-60 in Marchant teaches that the recorded code is a cross interleaved code so that Figures 5-7 shows how the inner codewords line up with scratches on a recording media prior to being read and processed to recover the stored data hence prior to being de-interleaved); configuring erasure position information of said first byte of main data belonging to the error correction target code line to be identical to erasure position information of said second byte of main data belonging to the previous error correction code line when said judging judges that the first byte of main data and the

second byte of main data were both located between the first and second bytes of sub data before being deinterleaved (col. 6, lines 28-56 in Marchant teach that symbols in a scratch field are configured/flagged with erasure information for a scratch so that they are configured/flagged with erasure position information for the same scratch, in particular; this process is a step for configuring/flagging erasure position information of said first piece of data 48b belonging to the outer/column error correction target code line 44b to be the same as identical row position 3 to erasure position information of said second piece of data 48a belonging to the previous error correction code line 44a when said judgment step judging judges that the first piece of data 48b and the second piece of data 48a are both located between the same pieces of inner/row codeword sub data rows 2 to 4), the erasure position information being obtained at a time of performing Reed-Solomon decoding on the Reed-Solomon-coded data (Col. 3, lines 41-47 in Marchant teaches that configuring/flagging with erasure position information occurs during inner decoding; Note: in cross interleaved codewords, inner decoding occurs before deinterleaving, e.g., Figure 2 in the Kobayashi teaching reference): and performing error correction on the error correction target code line (col. 6, lines 28-56 in Marchant).

As per additional limitations in claim 23: Col. 3, lines 41-47 in Marchant teaches that configuring/flagging with erasure position information occurs during inner decoding prior to de-interleaving.

However Marchant does not explicitly teach the specific use of erasure position information being obtained from a position polynomial. **Note: col. 3, lines 41-59 in**

Marchant teaches that C1 inner codeword rows exceeding error correction capabilities are flagged. An erasure flagged row within a C2 column outer code codeword is a position of an erroneous symbol within the C2 column outer code codeword. Hence, the erasure flag in Marchant provides error position information for a symbol within a C2 column/outer code codeword.

Nakamura, in an analogous art, teaches the erasure position information being obtained from a position polynomial (Col. 6, line 51 to col. 7, line 9 and Figure 5 in Nakamura teaches that during C1 inner decoding error location/position polynomials are generated in Block 3 and are used to generate feedback information to generate erasure information in Blocks 7, 7(b), 7(c) and 8; Specifically, col. 7, lines 2-5 in Nakamura teaches that error locations of the C1 inner/row error location/position polynomial are converted to erasure locations to be used in C2 outer/column error correction decoding whenever uncorrectable-error flags are output to Blocks 7, 7(b), 7(c) and 8, that is: the erasure position/location information stored in Block 8 is obtained from a error/position polynomial).

In summary, col. 6, line 61 to col. 7, line 8 in Nakamura teach that error locations of the C1 inner/row error location/position polynomial are converted to erasure locations to be used in C2 outer/column error correction decoding whenever uncorrectable-error flags are output to Blocks 7, 7(b), 7(c) and 8, which is substantially what is already taught in Marchant. Col. 6, line 6-17 of Marchant clearly suggests the use of a Reed-Solomon Erasure code. Nakamura teaches that in Reed-Solomon Erasure decoding erasures are erasure flagged during C1

inner/row code decoding just as in Marchant. However, Nakamura provides details missing in Marchant as to how erasure flagging is executed. Col. 6, line 51 to col. 7, line 9 and Figure 5 in Nakamura teaches that during C1 inner decoding error location/position polynomials are generated in Block 3 and are used to generate feedback information to generate erasure information in Blocks 7, 7(b), 7(c) and 8. Specifically, col. 7, lines 2-5 in Nakamura teaches that error locations of the C1 inner/row error location/position polynomial are converted to erasure locations to be used in C2 outer/column error correction decoding whenever uncorrectable-error flags are output to Blocks 7, 7(b), 7(c) and 8, that is: the erasure position/location information stored in Block 8 is obtained from a error/position polynomial).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Marchant with the teachings of Nakamura by including use of erasure position information being obtained from a position polynomial. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of erasure position information being obtained from a position polynomial would have provided a means for obtaining erasure information for inner C1 uncorrectable errors (col. 6, line 51 to col. 7, line 9 and Figure 5 in Nakamura).

However Marchant does not explicitly teach the specific use of a typical DVD recording data structure as encompassed in the language "wherein the ECC block includes a plurality of main data areas comprising the plurality of bytes of main data of the error

correction target code line and the plurality of bytes of main data of the previous error correction target code line, and a plurality of sub data areas comprising the plurality of bytes of sub data, wherein the plurality of main data areas include a first main data area and a second main data area, wherein the plurality of sub data areas include: a first sub data area in which the first byte of sub data is located; a second sub data area in which the second byte of sub data is located; and a third sub data area in which a third byte of sub data is located, wherein the first main data area is disposed between the first sub data area and the second sub data area, wherein the second main data area is disposed between the second sub data area and the third sub data area wherein the second sub data area is disposed between the first main data area and the second main data area, and wherein said error correction target code line extends so as to be located in both of the first and second main data areas of the ECC block".

Shutoku, in an analogous art, teaches use of a typical DVD recording data structure as encompassed in the language "wherein the ECC block includes a plurality of main data areas comprising the plurality of bytes of main data of the error correction target code line and the plurality of bytes of main data of the previous error correction target code line, and a plurality of sub data areas comprising the plurality of bytes of sub data, wherein the plurality of main data areas include a first main data area and a second main data area, wherein the plurality of sub data areas include: a first sub data area in which the first byte of sub data is located; a second sub data area in which the second byte of sub data is located; and a third sub data area in which a third byte of sub data is located, wherein the first main data area is disposed between the first sub data area

and the second sub data area, wherein the second main data area is disposed between the second sub data area and the third sub data area wherein the second sub data area is disposed between the first main data area and the second main data area, and wherein said error correction target code line extends so as to be located in both of the first and second main data areas of the ECC block" (Figure 1-3 and col. 8, lines 52-55 in Shutoku).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Marchant with the teachings of Shutoku by including use of a typical DVD recording data structure as encompassed in the language "wherein the ECC block includes a plurality of main data areas comprising the plurality of bytes of main data of the error correction target code line and the plurality of bytes of main data of the previous error correction target code line, and a plurality of sub data areas comprising the plurality of bytes of sub data, wherein the plurality of main data areas include a first main data area and a second main data area, wherein the plurality of sub data areas include: a first sub data area in which the first byte of sub data is located; a second sub data area in which the second byte of sub data is located; and a third sub data area in which a third byte of sub data is located, wherein the first main data area is disposed between the first sub data area and the second sub data area, wherein the second main data area is disposed between the second sub data area and the third sub data area wherein the second sub data area is disposed between the first main data area and the second main data area, and wherein said error correction target code line extends so as to be located in both of the first and second main data areas of the ECC

block". This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of a typical DVD recording data structure as encompassed in the language "wherein the ECC block includes a plurality of main data areas comprising the plurality of bytes of main data of the error correction target code line and the plurality of bytes of main data of the previous error correction target code line, and a plurality of sub data areas comprising the plurality of bytes of sub data, wherein the plurality of main data areas include a first main data area and a second main data area, wherein the plurality of sub data areas include: a first sub data area in which the first byte of sub data is located; a second sub data area in which the second byte of sub data is located; and a third sub data area in which a third byte of sub data is located, wherein the first main data area is disposed between the first sub data area and the second sub data area, wherein the second main data area is disposed between the second sub data area and the third sub data area wherein the second sub data area is disposed between the first main data area and the second main data area, and wherein said error correction target code line extends so as to be located in both of the first and second main data areas of the ECC block" would have provided scratch protection for DVDs.

35 U.S.C. 103(a) rejection of claims 37 and 38.

Marchant teaches an error correction method for an error correction code (ECC) block that includes Reed-Solomon-coded data said error correction method using a plurality of bytes of sub data which comprise error correction codes that are independent from error

correction codes of an error correction target code line to configure erasure position information (col. 3, lines 30-59 in Marchant teaches using a plurality of pieces of inner/row codeword sub data which comprise error correction codes that are independent from error correction codes of an outer/column error correction target code line to configure erasure position information; Note: col. 3, lines 41-57 in Marchant teaches that inner/row codeword sub data of the product code is used to configure erasure position information),

the plurality of bytes of sub data including at least a first byte of sub data and a second byte of sub data (Figure 7 of Marchant teaches that the plurality of bytes of sub data include at least a first byte of sub data 48b in inner/row codeword sub data row 3 of Figure 7 and a second byte of sub data 48a in inner/row codeword sub data row 3), said error correction method comprising:

judging whether or not a first byte of main data, which is one of a plurality of bytes of main data of the error correction target code line, and a second byte of main data, which is one of a plurality of bytes of main data of a previous error correction code line, were located between the first and second bytes of sub data before being deinterleaved (col. 6, lines 28-56 in Marchant teach judging whether or not a first piece of data 48b in inner/row codeword sub data row 3 of Figure 7, which is one of a plurality of pieces of data of the outer/column error correction target code line 44b, and a second piece of data 48a in inner/row codeword sub data row 3, which is one of a plurality of pieces of data of a previous error correction code line 44a, were located between the same pieces of inner/row codeword sub data rows 2 to 4 before being deinterleaving; Note:

Col. 4, lines 41-60 in Marchant teaches that the recorded code is a cross interleaved code so that Figures 5-7 shows how the inner codewords line up with scratches on a recording media prior to being read and processed to recover the stored data hence prior to being de-interleaved); configuring erasure position information of said first byte of main data belonging to the error correction target code line to be identical to erasure position information of said second byte of main data belonging to the previous error correction code line when said judging judges that the first byte of main data and the second byte of main data were both located between the first and second bytes of sub data before being deinterleaved (col. 6, lines 28-56 in Marchant teach that symbols in a scratch field are configured/flagged with erasure information for a scratch so that they are configured/flagged with erasure position information for the same scratch, in particular; this process is a step for configuring/flagging erasure position information of said first piece of data 48b belonging to the outer/column error correction target code line 44b to be the same as identical row position 3 to erasure position information of said second piece of data 48a belonging to the previous error correction code line 44a when said judgment step judging judges that the first piece of data 48b and the second piece of data 48a are both located between the same pieces of inner/row codeword sub data rows 2 to 4), the erasure position information being obtained at a time of performing Reed-Solomon decoding on the Reed-Solomon-coded data (Col. 3, lines 41-47 in Marchant teaches that configuring/flagging with erasure position information occurs during inner decoding; Note: in cross interleaved codewords, inner decoding occurs before deinterleaving, e.g., Figure 2 in the Kobayashi teaching reference): and

performing error correction on the error correction target code line (col. 6, lines 28-56 in Marchant).

Sub data 48a and 48b in Figure 7 of Marchant is sync data for configuring/flagging erasures.

As per additional limitations in claim 38: Col. 3, lines 41-47 in Marchant teaches that configuring/flagging with erasure position information occurs during inner decoding prior to de-interleaving.

However Marchant does not explicitly teach the specific use of erasure position information being obtained from a position polynomial. **Note: col. 3, lines 41-59 in Marchant teaches that C1 inner codeword rows exceeding error correction capabilities are flagged. An erasure flagged row within a C2 column outer code codeword is a position of an erroneous symbol within the C2 column outer code codeword. Hence, the erasure flag in Marchant provides error position information for a symbol within a C2 column/outer code codeword.**

Nakamura, in an analogous art, teaches the erasure position information being obtained from a position polynomial **(Col. 6, line 51 to col. 7, line 9 and Figure 5 in Nakamura teaches that during C1 inner decoding error location/position polynomials are generated in Block 3 and are used to generate feedback information to generate erasure information in Blocks 7, 7(b), 7(c) and 8; Specifically, col. 7, lines 2-5 in Nakamura teaches that error locations of the C1 inner/row error location/position polynomial are converted to erasure locations to be used in C2 outer/column error correction decoding whenever uncorrectable-error flags are output to**

Blocks 7, 7(b), 7(c) and 8, that is; the erasure position/location information stored in Block 8 is obtained from a error/position polynomial).

In summary, col. 6, line 61 to col. 7, line 8 in Nakamura teach that error locations of the C1 inner/row error location/position polynomial are converted to erasure locations to be used in C2 outer/column error correction decoding whenever uncorrectable-error flags are output to Blocks 7, 7(b), 7(c) and 8, which is substantially what is already taught in Marchant. Col. 6, line 6-17 of Marchant clearly suggests the use of a Reed-Solomon Erasure code. Nakamura teaches that in Reed-Solomon Erasure decoding erasures are erasure flagged during C1 inner/row code decoding just as in Marchant. However, Nakamura provides details missing in Marchant as to how erasure flagging is executed. Col. 6, line 51 to col. 7, line 9 and Figure 5 in Nakamura teaches that during C1 inner decoding error location/position polynomials are generated in Block 3 and are used to generate feedback information to generate erasure information in Blocks 7, 7(b), 7(c) and 8. Specifically, col. 7, lines 2-5 in Nakamura teaches that error locations of the C1 inner/row error location/position polynomial are converted to erasure locations to be used in C2 outer/column error correction decoding whenever uncorrectable-error flags are output to Blocks 7, 7(b), 7(c) and 8, that is; the erasure position/location information stored in Block 8 is obtained from a error/position polynomial).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Marchant with the teachings of Nakamura by including

use of erasure position information being obtained from a position polynomial. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of erasure position information being obtained from a position polynomial would have provided a means for obtaining erasure information for inner C1 uncorrectable errors (col. 6, line 51 to col. 7, line 9 and Figure 5 in Nakamura).

However Marchant does not explicitly teach the specific use of a typical DVD recording data structure as encompassed in the language "wherein the ECC block includes a plurality of main data areas comprising the plurality of bytes of main data of the error correction target code line and the plurality of bytes of main data of the previous error correction target code line, and a plurality of sub data areas comprising the plurality of bytes of sub data, wherein the plurality of main data areas include a first main data area and a second main data area, wherein the plurality of sub data areas include: a first sub data area in which the first byte of sub data is located; a second sub data area in which the second byte of sub data is located; and a third sub data area in which a third byte of sub data is located, wherein the first main data area is disposed between the first sub data area and the second sub data area, wherein the second main data area is disposed between the second sub data area and the third sub data area wherein the second sub data area is disposed between the first main data area and the second main data area, and wherein said error correction target code line extends so as to be located in both of the first and second main data areas of the ECC block".

Shutoku, in an analogous art, teaches use of a typical DVD recording data structure as encompassed in the language "wherein the ECC block includes a plurality of main data areas comprising the plurality of bytes of main data of the error correction target code line and the plurality of bytes of main data of the previous error correction target code line, and a plurality of sub data areas comprising the plurality of bytes of sub data, wherein the plurality of main data areas include a first main data area and a second main data area, wherein the plurality of sub data areas include: a first sub data area in which the first byte of sub data is located; a second sub data area in which the second byte of sub data is located; and a third sub data area in which a third byte of sub data is located, wherein the first main data area is disposed between the first sub data area and the second sub data area, wherein the second main data area is disposed between the second sub data area and the third sub data area wherein the second sub data area is disposed between the first main data area and the second main data area, and wherein said error correction target code line extends so as to be located in both of the first and second main data areas of the ECC block" (Figure 1-3 and col. 8, lines 52-55 in Shutoku).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Marchant with the teachings of Shutoku by including use of a typical DVD recording data structure as encompassed in the language "wherein the ECC block includes a plurality of main data areas comprising the plurality of bytes of main data of the error correction target code line and the plurality of bytes of main data of the previous error correction target code line, and a plurality of sub data areas

comprising the plurality of bytes of sub data, wherein the plurality of main data areas include a first main data area and a second main data area, wherein the plurality of sub data areas include: a first sub data area in which the first byte of sub data is located; a second sub data area in which the second byte of sub data is located; and a third sub data area in which a third byte of sub data is located, wherein the first main data area is disposed between the first sub data area and the second sub data area, wherein the second main data area is disposed between the second sub data area and the third sub data area wherein the second sub data area is disposed between the first main data area and the second main data area, and wherein said error correction target code line extends so as to be located in both of the first and second main data areas of the ECC block". This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of a typical DVD recording data structure as encompassed in the language "wherein the ECC block includes a plurality of main data areas comprising the plurality of bytes of main data of the error correction target code line and the plurality of bytes of main data of the previous error correction target code line, and a plurality of sub data areas comprising the plurality of bytes of sub data, wherein the plurality of main data areas include a first main data area and a second main data area, wherein the plurality of sub data areas include: a first sub data area in which the first byte of sub data is located; a second sub data area in which the second byte of sub data is located; and a third sub data area in which a third byte of sub data is located, wherein the first main data area is disposed between the first sub data area and the second sub data

area, wherein the second main data area is disposed between the second sub data area and the third sub data area wherein the second sub data area is disposed between the first main data area and the second main data area, and wherein said error correction target code line extends so as to be located in both of the first and second main data areas of the ECC block” would have provided scratch protection for DVDs.

Claims 21 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Marchant; Alan B. (US 6631492 B2) in further view of Nakamura; Takahiko et al. (US 5684810 A, hereafter referred to as Nakamura) and Kobayashi; Hisashi et al. (US 6029264 A, hereafter referred to as Kobayashi; Note: Kobayashi is used strictly as a teaching reference) in further view of Eachus; Joseph J. (US 3685016 A).

35 U.S.C. 103(a) rejection of claims 21 and 26.

Marchant and Nakamura substantially teach the claimed invention described in claims 17-20, 22-25, 27-30 and 32-35 (as rejected above).

However Marchant and Nakamura do not explicitly teach the specific use of avoiding error correction when error correction capabilities are exceeded.

Eachus, in an analogous art, teaches use of avoiding error correction when error correction capabilities are exceeded (col. 13, lines 1-10 in Eachus).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Marchant and Nakamura with the teachings of Eachus by including use of avoiding error correction when error correction capabilities are

exceeded. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of avoiding error correction when error correction capabilities are exceeded would have provided means for avoiding meaningless calculations (col. 13, lines 1-10 in Eachus).

#### **(10) Response to Argument**

Summary of Inner and Outer codes of a product codes as they relate to the Prior Art: Generally, Inner and Outer codes of a product code refer to a pair of serially concatenated codes whereby the outer code is encoded prior to encoding the inner code and whereby the inner code is decoded prior to decoding the outer code, that is, decoding is done in the reverse direction. For example, Figure 7 in Nakamura (US 5684810 A) clearly suggests that that the C1 row code portion of the product code in Figure 22 is an inner code and that the C2 column code portion of the product code in Figure 22 is an outer code. Since col. 5, lines 3-5 in Marchant teaches that Figure 5 is directed to transverse ECC codes and col. 6, lines 24-27 in Marchant teaches that the transverse ECC code is a product code comprising inner and outer codewords, the combination of Marchant and Nakamura teach product codes comprising C1 inner/row codes and C2 outer/column codes. **Marchant teaches the use of supplemental Scratch detection field information for use in erasure correction decoding to improve error correction capabilities for the erasure correction decoding process of a product code comprising C1 inner/row codes and C2 outer/column codes**

(col. 6, lines 40-56 in Marchant) whereas Nakamura teaches well-known elements of **erasure correction decoding processes of product codes comprising C1 inner/row codes and C2 outer/column codes** that Marchant intended and took for granted (see col. 6, line 51 to col. 7, line 9 and Figure 5 in Nakamura).

On pages 10-11, Section I of the Appellant's Appeal brief, the Appellant contends, "Appellants note that Figs. 5-7 in Marchant do not relate to a product code, and therefore, Appellants submit that there is clearly no concept of "decoding of C1 inner/row code" in these figures of Marchant."

In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

The Examiner asserts col. 5, lines 3-5 in Marchant teaches that Figure 5 is directed to transverse ECC codes and col. 6, lines 24-27 in Marchant teaches that the transverse ECC code is a product code comprising inner and outer codewords. Figure 7 in Nakamura (US 5684810 A) clearly suggests that that the C1 row code portion of the product code in Figure 22 is an inner code and that the C2 column code portion of the product code in Figure 22 is an outer code. Since col. 5, lines 3-5 in Marchant teaches Figure 5 is directed to transverse ECC codes and col. 6, lines 24-27 in Marchant teaches that the transverse ECC code is a product code comprising inner and outer

codewords, the combination of Marchant and Nakamura teach product codes comprising C1 inner/row codes and C2 outer/column codes.

On page 11, Section I of the Appellant's Appeal brief, the Appellant contends, "Appellants note that while Figs. 5-7 of Marchant perform detection of erasure by scratch detection fields (e.g., see col. 6, lines 28-56 of Marchant), that Figs. 5-7 of Marchant do not perform detection of erasure by inner code".

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., "perform detection of erasure by inner code") are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Claim 17 instead recites, "the erasure position information being obtained from a position polynomial that is calculated at a time of performing Reed-Solomon decoding on the Reed-Solomon-coded data"

Column 6, lines 47-52 in Marchant teaches that **Scratch detection fields** are provided at a minimum spatial frequency such that each transverse ECC code word symbol is bracketed by scratch detection symbols on the same data track and a plurality of ECC code word symbols are recorded between consecutive scratch detection symbols on the same data track and col. 6, lines 51-56 in Marchant clearly suggest that the **Scratch detection fields** are then submitted for erasure correction processing where error

locations within a codeword can be found and corrected (Note: the exact location of erasure symbols within the product code is unknown prior to erasure correction decoding since, as col. 6, lines 40-45 in Marchant teach, ECC code word symbol bracketed between **Scratch detection fields** are only suspect scratch locations submitted for erasure correction processing where error locations within a codeword can be found and corrected), **hence Marchant teaches the use of supplemental Scratch detection field information to improve error correction capabilities during erasure correction decoding of a product codes comprising C1 inner/row codes and C2 outer/column codes.** Marchant does not teach each and every element of erasure correction decoding since erasure correction decoding is well known in the art (e.g., see Nakamura). Nakamura teaches well-known elements of erasure correction decoding, and in particular, col. 6, line 51 to col. 7, line 9 and Figure 5 in Nakamura teaches that during C1 inner decoding error location/position polynomials are generated in Block 3 and are used to generate feedback information to generate erasure information in Blocks 7, 7(b), 7(c) and 8. Specifically, col. 7, lines 2-5 in Nakamura teaches that error locations of the C1 inner/row error location/position polynomial are converted to erasure locations to be used in C2 outer/column error correction decoding whenever uncorrectable-error flags are output to Blocks 7, 7(b), 7(c) and 8, that is; the erasure position/location information stored in Block 8 is obtained from an error/position polynomial.

On page 11, Section I of the Appellant's Appeal brief, the Appellant contends, "Thus, because Marchant merely performs detection of erasure by scratch detection fields, Appellants submit that it would be impossible to combine Figs. 5-7 of Marchant, which do not relate to the product code, with Nakamura, which relates to a decoding method for decoding the product code comprising the inner code and the outer code. In other words, Appellants submit that because Marchant performs detection of erasure by scratch detection fields, and does not perform detection of erasure by inner code, that combining Marchant and Nakamura in the manner suggested by the Examiner would render Marchant either inoperable, or unsatisfactory, for its intended principle of operation, which is performing detection of erasure by scratch detection fields."

The Examiner disagrees and asserts col. 5, lines 3-5 in Marchant teaches that Figure 5 is directed to transverse ECC codes and col. 6, lines 24-27 in Marchant teaches that the transverse ECC code is a product code comprising inner and outer codewords.

**Marchant teaches the use of supplemental Scratch detection field information for use in erasure correction decoding to improve error correction capabilities for the erasure correction decoding process of a product code comprising C1 inner/row codes and C2 outer/column codes** whereas Nakamura teaches well-known elements of **erasure correction decoding processes of product codes comprising C1 inner/row codes and C2 outer/column codes** that Marchant intended and took for granted.

**(11) Related Proceeding(s) Appendix**

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

/Joseph D Torres/

Primary Examiner, Art Unit 2112

Conferees:

/Scott Baderman/

Supervisory Primary Examiner, Art Unit 2112

/MUJTABA K CHAUDRY/

Primary Examiner, Art Unit 2112